CLAIMS

What is claimed is:

1. A system for merging a plurality of connections that share a same class of service into a single virtual circuit (VC) connecting a first switching node to a second switching node in an Asynchronous Transfer Mode (ATM) network, said system comprising:

a data buffer for storing cells that constitute a packet received by a switching node;

a queuing apparatus comprising:

a plurality of connection queues associated respectively with each of said plurality of connections; and

a scheduled queue corresponding to a particular class of service, wherein contents of said plurality of connection queues are transferred into said scheduled queue before being transmitted on said VC;

a reassembly queue control block (RQCB) associated with each of said plurality of connection queues, wherein said RQCB defines a chain of buffer control blocks, wherein each buffer control block corresponds to a cell belonging to a packet transmitted in a particular connection, and wherein said buffer control block includes a next buffer address in said data buffer and a lock bit that is normally set to 1 for an incoming cell and is set to 0 for an

incoming cell only if said incoming cell is a last cell of said packet; and

a scheduled queue control block (SQCB) associated with said scheduled queue to which said chain of buffer control blocks is transferred in response to a determination that said lock bit of a cell stored within said data buffer is set to 0, wherein a corresponding buffer control block is chained to said chain of buffer control blocks in said SQCB without having been previously queued in said RQCB.

2. The system of claim 1, wherein said plurality of connections includes several sets of connections wherein each set of connections is associated with different classes of service, and further comprising a merged VC scheduler for scheduling a transmission of cells from said scheduled queues that are respectively associated with said alternate SQCBs in accordance with said different classes of service.

3. The system of claim 2, wherein said merged VC scheduler includes processing means for scheduling cell transmission based upon a priority order of said different classes of service.

4. The system of claim 3, further comprising locking means for locking cell transmission from a scheduled queue associated with a SQCB until said scheduled queue has received a last cell of an entire packet.

5. The system of claim 4, wherein said locking means unlocks said merged VC scheduler in response to a lock bit

of a buffer control block that corresponds to a cell to be transmitted is set to 0.

6. The system of claims 1, further comprising an aging mechanism that is periodically activated for discarding cells that are currently enqueued in a queue associated with a RQCB in response to no cell having been enqueued in said RQCB during a predetermined period of time.

7. The system of claim 6, wherein said RQCB further includes an aging bit, wherein said aging bit being automatically set to 0 in response to a first cell being enqueued in said RQCB.

8. The system of claim 7, further comprising:

processing means for periodically activating said aging mechanism being to discard cells enqueued in said RQCB in response to said aging bit being set to 1; and

processing means for setting said aging bit to 1 in response to said aging bit being previously set to 0.

9. The system of claim 1, further comprising a connection control block is associated with each connection to be merged within said VC, wherein said connection control block includes an address of a RQCB utilized to assemble packets corresponding to said connection.

10. The system of claim 9, wherein said connection control block further comprises processing means for enqueueing cells corresponding to said RQCB in accordance with an address of a SQCB associated with said connection.

11. The system of claim 9, wherein said connection control block further includes a discard flag bit for indicating that a packet in progress is being discarded.

12. The system of claim 11, further comprising an early packet discard processing means for setting said discard flag bit in said connection control block in response to activation of said connection control block and for discarding cells of an incoming packet in response to said early packet discard means being activated prior to said connection control block receiving a first cell of said incoming packet.

13. The system of claim 11, further comprising a partial packet discard processing means for setting said discard flag bit in response to activation of said connection control block, and for purging said RQCB by deleting the presently enqueued and following cells of an incoming packet.